Hall Ticket Number:

Code No. : 14448

VASAVI COLLEGE OF ENGINEERING *(AUTONOMOUS)*, HYDERABAD

Accredited by NAAC with A++ Grade

B.E. (E.C.E.) IV-Semester Main & Backlog Examinations, August-2022

Computer Organization and Architecture

Time: **3 hours** Max. Marks: **60**

*Note: Answer all questions from **Part-A** and any **FIVE** from **Part-B***

Part-A (10 × 2 = 20 Marks)

Q. No.	Stem of the question	M	L	CO	PO
1.	If 11 bits are used for the representation of a number in 2's complement, what will be the maximum number in signed number range? Justify your answer.	2	3	1	2
2.	Differentiate between 3rd and 4th Computer Generations	2	2	1	1
3.	List the Functions of a Microprogram Sequencer?	2	1	2	1
4.	Write the content of the flag register of 8085 after executing the following operation : (5Bh + F9h)	2	3	2	2
5.	Compare any four Characteristics of CISC and RISC CPU cores?	2	1	3	1
6.	Define Amdahl's Law and list the consequences of Amdahl's law?	2	2	3	2
7.	Draw the interface diagram for CPU with DMA Controller showing the sequence of control signals?	2	1	4	1
8.	Represent the frame format to transfer the character "A" over an Asynchronous channel that includes 1 - start bit of High pulse, 2 - stop bits of low pulse and 1- high pulse for parity?	2	3	4	2
9.	Define memory Hierarchy? Represent the Pyramid structure of Memory hierarchy?	2	3	5	1
10.	Write any four Features of Associative memory?	2	1	5	2
	Part-B (5 × 8 = 40 Marks)				
11. a)	Perform the Multiplication of given floating point numbers 3.45×10^{-2} and 0.2×10^{-1}. Normalize the result and express in IEEE standard?	3	1	1	1
b)	What is the drawback in parallel adder circuit? Explain with suitable justification how the look ahead carry generator circuit overcomes the drawback of parallel adder circuit?	5	2	1	2
12. a)	Explain the operation of the following pins of 8085 CPU a) ALE b) INTR c) NMI d) HOLD	4	2	2	1

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b)	Explain the Operation of hardwired Control unit of a basic computer with suitable diagram?	4	2	2	2
13. a)	A non-pipeline system takes 60ns to perform a task. The same task can be processed in a six-segment pipeline with a clock cycle of 10ns. Determine the speed up ratio of the pipeline for 100 tasks. What is the maximum speedup that can be achieved?	3	4	3	2
b)	Explain the operation of SIMD array processor with a suitable diagram?	5	1	3	1
14. a)	Design a parallel priority encoder interrupt circuit considering 8 different interrupt sources?	5	4	4	2
b)	What is the necessity of an Asynchronous I/O interface Circuit?	3	2	4	1
15. a)	A computer employs RAM chips of 1024 x 8 and ROM chips of 512 x 8. The computer system needs 2K bytes of RAM, 2K bytes of ROM. i) How many RAM and ROM chips are needed? ii) Daw a memory-address map for the system?	4	4	5	2
b)	Represent an Address relationship between main memory size of 1MB and cache memory size of 256 bytes? Explain about the Direct mapping cache organization for the above representation?	4	3	5	2
16. a)	Perform (-9) * (13) using Booth's Multiplication algorithm for Fixed point numbers? Demonstrate the execution with algorithmic steps?	5	3	1	1
b)	Discuss about the Interrupts of 8085 CPU?	3	2	2	1
17.	Answer any ***two*** of the following:				
a)	Define Pipeline Hazard? Explain any two methods to overcome structural hazard?	4	2	3	1
b)	Explain the CPU-IOP communication process with a suitable diagram?	4	2	4	1
c)	Explain any 2-page replacement algorithms adopted by the Memory management hardware?	4	2	5	1

M : Marks; L: Bloom's Taxonomy Level; CO; Course Outcome; PO: Programme Outcome

i)	Blooms Taxonomy Level – 1	20%
ii)	Blooms Taxonomy Level – 2	40%
iii)	Blooms Taxonomy Level – 3 & 4	40%

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